

Amendments to the Claims

Please cancel Claims 2 and 10. Please amend Claims 1, 3-4 and 9. The Claim Listing below will replace all prior versions of the claims in the application:

Claim Listing

1. (Currently Amended) A method of providing clock timing in a receiver, the method comprising:
 - providing a local clock signal having a reference frequency by dividing a local oscillator signal by a clock divisor having an initial nominal value;
 - receiving a stream of data cells in a receiver buffer;
 - servicing the receiver buffer to remove the data cells at a servicing rate based on the local clock signal;
 - monitoring fullness of the receiver buffer at a monitoring interval;
 - upon buffer fullness exceeding a high buffer threshold, adjusting the clock reference frequency upwards by setting the clock divisor to a value less than the nominal value and by stretching the local clock signal by half a cycle of the local oscillator signal;
 - upon buffer fullness dropping below a low buffer threshold, adjusting the clock reference frequency downwards by setting the clock divisor to the nominal value and by stretching the local clock signal by half a cycle of the local oscillator signal.
2. (Cancelled)
3. (Currently Amended) The method of Claim 1 further comprising: once the buffer fullness exceeds the high buffer threshold and upon buffer fullness dropping below a nominal threshold less than the high buffer threshold and greater than the low buffer threshold, adjusting the clock reference frequency downwards by setting the clock divisor to the nominal value without stretching the local clock signal by half a cycle of the local oscillator signal.

4. (Currently Amended) The method of Claim 1 further comprising: once the buffer fullness drops below the low buffer threshold and upon buffer fullness exceeding a nominal threshold less than the high buffer threshold and greater than the low buffer threshold, adjusting the clock reference frequency upwards by setting the clock divisor to the nominal value without stretching the local clock signal by half a cycle of the local oscillator signal.
5. (Original) The method of Claim 1 wherein the cell stream is an AAL1 stream and wherein the monitoring interval comprises a first number of ATM cell periods.
6. (Original) The method of Claim 5 wherein clock adjustment is made only if buffer fullness exceeds the high buffer threshold or drops below the low buffer threshold at each monitoring interval for a second number of consecutive monitoring intervals.
7. (Original) The method of Claim 1 wherein the cell stream includes cells from plural virtual circuits and receiving includes receiving cells from the plural virtual circuits in respective receiver buffers.
8. (Original) The method of Claim 7 further comprising selecting one of the plural virtual circuits and wherein monitoring includes monitoring fullness of the receiver buffer corresponding to the selected virtual circuit.
9. (Currently Amended) A receiver comprising:
 - a clock source for providing a local clock signal having a reference frequency by dividing a local oscillator signal by a clock divisor having an initial nominal value;
 - a receiver buffer for receiving a stream of data cells;
 - means for servicing the receiver buffer to remove the data cells at a servicing rate based on the local clock signal;
 - means for monitoring fullness of the receiver buffer at a monitoring interval;

means for adjusting the clock reference frequency upwards upon buffer fullness exceeding a high buffer threshold by setting the clock divisor to a value less than the nominal value and by stretching the local clock signal by half a cycle of the local oscillator signal and for adjusting the clock reference frequency downwards upon buffer fullness dropping below a low buffer threshold by setting the clock divisor to the nominal value and by stretching the local clock signal by half a cycle of the local oscillator signal.

10. (Cancelled)
11. (Original) The receiver of Claim 9 wherein the cell stream is an AAL1 stream and wherein the monitoring interval comprises a first number of ATM cell periods.
12. (Original) The receiver of Claim 11 wherein clock adjustment is made only if buffer fullness exceeds the high buffer threshold or drops below the low buffer threshold at each monitoring interval for a second number of consecutive monitoring intervals.
13. (Original) The receiver of Claim 9 wherein the receiver buffer comprises plural receiver buffers and wherein the cell stream includes cells from plural virtual circuits and the plural receiver buffers receive cells from respective virtual circuits.
14. (Original) The receiver of Claim 13 further comprising means for selecting one of the plural virtual circuits and wherein monitoring includes monitoring fullness of the receiver buffer corresponding to the selected virtual circuit.